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10/811,326	03/26/2004	Frank M. Cerio JR.	TAZ-259	9467

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
1795	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)
	10/811,326	CERIO ET AL.
	Examiner	Art Unit
	Rodney G. McDonald	1795

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,9-19,26-40,43,45-49,53,55,57-64,67-70,73,74,77-89 and 92-111* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1, 2, 6, 7, 9-19, 26-40, 43, 45-49, 53, 55, 57-64, 67-70, 73, 74, 77-89, 92-111

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 6, 7, 9-11, 13-19, 26-27, 30-33, 35-40, 92, 93, 94, 95 and 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al. (U.S. Pat. 6,051,114) in view of Yasar et al. (US PGPUB2003/0034244 A1).

Regarding claims 1, 92, Yao et al. teach a method of operating a deposition system comprising positioning a patterned substrate on a wafer table within a processing chamber. The patterned substrate has features such as a field area, a sidewall and a bottom surface. (See Fig. 1; (See Fig. 3A-3C; Column 5 lines 36-43) Creating a high density plasma in the processing chamber wherein the high density

plasma comprises ions of coating material and a large number of process gas ions. (Column 3lines 25-42; Column 6 lines 12-26) Exposing the patterned substrate to the high-density plasma. Performing a Low Net Deposition (LND) process wherein a target and substrate bias power is adjusted to establish an LND deposition rate. (Column 4 lines 7-18; Column 5 lines 44-68; Column 6 lines 1-27) The performing of the LND process step includes depositing material onto the field area at a deposition rate of not more than 30 nanometers per minute while depositing or etching material, or a combination thereof, on the sidewall or the bottom surface or a combination thereof and thereby producing substantially no overhanging material at feature openings. Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27) Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18)

Regarding claim 35, Yao et al. teach using an ionized physical vapor deposition chamber. (Column 6 lines 1-11)

Regarding claim 94, Yao et al. teach depositing a seed layer such as copper. (Column 5 line 2)

Regarding claim 95, Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27)

Regarding claim 96, Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18)

The differences between Yao et al. and the present claims is that the wafer table being cooled to a temperature of approximately -30 degrees C is not discussed (Claim

1), the LND processing time is not discussed (Claim 2), the power to the target is not discussed (Claim 9), the pressure during LND is not discussed (Claim 6), operating the ICP at a first frequency and adjusting the ICP source to provide an LND ICP power level for at least a portion of the LND processing time is not discussed (Claim 7), the LNP ICP power being 3000 w and less than approximately 6000 W is not discussed (Claim 7), the process gas during the LND process is not discussed (Claim 10), the gas being an inert gas is not discussed (Claim 11), depositing a barrier layer is not discussed (Claim 13), changing the process from an LND process to a No Net Deposition (NND) process comprising a field deposition rate, a sidewall deposition rate or a bottom surface deposition rate and controlling the chamber conditions to change the process form the LND process to the NND process (Claim 14), the NND deposition rate is not discussed (Claims 15-18), the NND processing time varying from 10 to 500 seconds is not discussed (Claim 19), the NND chamber pressure is not discussed (Claim 26), flowing a second process gas into the chamber for NND is not discussed (Claim 27), depositing a seed layer is not discussed (Claim 30), repairing a seed layer is not discussed (Claim 31), repairing a barrier layer is not discussed (Claim 32) depositing a barrier layer is not discussed (Claim 33), the deposition system comprising a transfer system is not discussed (Claim 36), performing a second LND process is not discussed (claim 37), utilizing a second chamber for a second LND process is not discussed (Claim 38), performing a second NND process is not discussed (claim 39), performing a second NND process in a second chamber is not discussed (Claim 40), and depositing a barrier layer is not discussed (claim 93).

Regarding claim 1, Yasar et al. teach the wafer and thus the wafer table to about -30 degrees C. (Paragraph 0039; Paragraph 0032)

Regarding claim 2, Yasar et al. teach the processing time for deposition can be between 10 and 500 seconds. (See Fig. 5)

Regarding claim 9, Yasar et al. teach low power applied to the sputtering target. (Paragraph 0006)

Regarding claim 6, Yasar et al. teach the pressure during the LND process can be 50-120 mT. (Table I)

Regarding claim 7, Yasar et al. teach operating RF power at a first frequency and adjusting the power to the ICP source. (See paragraph 0061; Table 1)

Regarding claim 7, Yasar et al. teach the ICP power during deposition is 1-7 kW. (See Table 1)

Regarding claim 10, Yasar et al. teach the sputtering gas can be argon gas and nitrogen. (Paragraph 0034)

Regarding claim 11, Yasar et al. teach the sputtering gas can be argon gas. (Paragraph 0034)

Regarding claim 13, Yasar et al. teach depositing a barrier layer. (See Paragraph 0034)

Regarding claim 14, Yasar et al. teach changing from a LND process to a NND process (i.e. an etching process) by adjusting chamber conditions. (See Paragraph 0035)

Regarding claims 15-18, Yasar et al. teach that the deposition rate can be 0 or lower since the deposition can be stopper. (Paragraph 0035)

Regarding claim 19, Yasar et al. teach that the NND process (i.e. etch) is between 10 to 500 seconds. (Fig. 5)

Regarding claim 26, Yasar et al. teach the chamber pressure to be 50-120 mT (See Table I) Yao et al. suggest that for a given target, substrate geometry, type of inert gas, target material and barrier layer an optimum pressure regime can be determined. Thus the pressure during NND can be greater than approximately 20 mT. (Column 4 lines 58-65)

Regarding claim 27, Yasar et al. teach utilizing nitrogen during deposition and argon during etching. (Paragraph 0034, 0035)

Regarding claims 30, 31, Yasar et al. teach depositing a seed layer or repairing a seed layer since the material is continually deposited. (See Paragraph 0031)

Regarding claims 32, 33, Yasar et al. teach depositing a barrier layer or repairing the barrier layer. (See Paragraph 0035)

Regarding claim 36, Yasar et al. teach utilizing a transfer system to transfer a substrate to a deposition system. (Paragraph 0007)

Regarding claim 37, Yasar et al. suggest depositing a barrier layer and then a seed layer on a substrate. (See Paragraph 0003; 0004) Yasar et al. suggest utilizing the deposition and etch process to deposit these layers. (See Paragraph 0011)

Regarding claim 38, Yasar et al. teach utilizing multiple deposition chambers for depositing layers. (Paragraph 0007)

Regarding claim 39, Yasar et al. suggest depositing a barrier layer and then a seed layer on a substrate. (See Paragraph 0003; 0004) Yasar et al. suggest utilizing the deposition and etch process to deposit these layers. (See Paragraph 0011)

Regarding claim 40, Yasar et al. teach utilizing a second chamber for a second NND process. (See Paragraph 0007)

Regarding claim 93, Yasar et al. teach depositing a barrier layer. (See paragraph 0035)

The motivation for utilizing the features of Yasar et al. is that it allows for metallization of high aspect ratio vias. (Paragraph 0002)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Yao et al. by utilizing the features of Yasar et al. because it allows for metallization of high aspect ratio vias.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al. in view of Yasar et al. as applied to claims 1-2, 6, 7, 9-11, 13-19, 26-27, 30-33, 35-40, 92, 93, 94, 95 and 96 above, and further in view of Konishi et al. (Japan 09-360040).

The differences not yet discussed is the metal gas. (Claim 12)

Regarding claim 12, Konishi et al. teach utilizing an organometallic gas during sputtering comprising Titanium. (See Konishi Abstract; Machine Translation)

The motivation for utilizing the features of Konishi et al. is that it allows for controlling the composition of the deposited film. (See Konishi et al. Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the features of Konishi et al. because it allows for controlling the composition of the deposited film.

Claim 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al. in view of Yasar et al. as applied to claims 1-2, 6, 7, 9-11, 13-19, 26-27, 30-33, 35-40, 92, 93, 94, 95 and 96 above, and further in view of Gopalraja et al. (U.S. Pat. 6,274,008).

The differences not yet discussed is punch through. (Claim 34)

Regarding claim 34, Gopalraja et al. teach punching through the bottom layer. (Column 13 lines 20-22)

The motivation for utilizing the features of Gopalraja et al. is that it allows for enhancing sidewall coverage. (Column 13 lines 22-23)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the features of Gopalraja et al. because it allows for enhancing sidewall coverage.

Claims 43, 45-49, 53, 55, 57-59, 61, 62, 84 and 97 and 64, 67-70, 73, 74, 77-79, 81-83, 85-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasar et al. (US PGPUB 2003/0034244 A1) in view of Yao et al. (U.S. Pat. 6,051,114).

Regarding claim 43, Yasar et al. teach a method of operating a deposition system by positioning a patterned substrate on a wafer table within a processing chamber. (See Figs. 3, 3A, 3B) Creating a high density plasma in the processing chamber wherein the high density plasma comprises a large concentration of metal ions

and a large number of process gas ions. Exposing the patterned substrate to the high density plasma. Performing a NO Net Deposition (NND) process, wherein a target power or a substrate bias power or a combination thereof, is adjusted to establish an NND deposition rate, the NND deposition rate comprising an NND field deposition rate, an NND sidewall deposition rate, or an NND bottom surface deposition rate or a combination thereof. Processing the patterned substrate using the NND process, thereby depositing material on sidewalls of features of the patterned substrate or bottom surfaces of features of the patterned substrate, or a combination thereof, wherein a chamber pressure, chamber temperature, substrate temperature, a process gas chemistry, a process gas flow rate, a target material, an ICP power, substrate position, a target power, or a substrate bias power, or a combination thereof, is adjusted during the NND process. (Paragraph 0035; Paragraph 0042; Paragraph 0043)

Regarding claim 48, Yasar et al. teach the NND time processing time can be between 10 to 500 seconds. (Fig. 5, 5B)

Regarding claim 49, Yasar et a. teach the NND time can be greater than approximately 150 seconds depending on the number of etch and deposition steps. (See Fig. 5)

Regarding claim 53, Yasar et al. teach the system includes a target 25 coupled to the wall, a permanent magnet pack coupled to the target, and a DC power source coupled to the target. (See Fig. 3; Paragraph 0032) The target power is substantially reduced therefore suggesting approximately 100 W to approximately 1500 W. (See Paragraph 0035)

Regarding claim 55, Yasar et al. teach the ICP source can be operated at a first frequency and adjusted. (Paragraph 0042; Paragraph 0061)

Regarding claim 57, Yasar et al. the ICP power can be 3000 W. (See Table II)

Regarding claim 58, Yasar et al. teach flowing a first process gas during the NND process. (Paragraph 0035)

Regarding claim 59, Yasar et al. teach the gas to be argon. (Paragraph 0035)

Regarding claims 61, 62, Yasar et al. teach depositing a barrier layer or repairing a barrier layer since the material continually deposits. (Paragraph 0034)

Regarding claim 84, Yasar et al. teach the deposition comprises a physical vapor deposition processing chamber. (See Fig. 3A)

Regarding claim 97, Yasar et al. teach simultaneous deposition and etching where the power is reduced to a low level of a low level deposit. (See Paragraph 0035; Paragraph 0012)

The differences between Yasar et al. and the present claims is that the wafer table is cooled to a temperature of approximately -30 degrees C is not discussed (Claim 43), the chamber pressure being 50-100 mTorr is not discussed (Claim 43), the target power level is not discussed (Claim 43), simultaneously directing ions of the material and ions of inert processing gas onto the substrate and thereby simultaneously depositing material onto the field are of the substrate while etching the deposited material from the field are of the substrate is not discussed (Claim 43), the deposition rate is not discussed (Claim 43, 45-47), changing the process from a NND process to a LND process where material is deposited on a field area of the substrate, sidewalls of

patterned features, or bottom features or combinations thereof, while producing no substantial overhanging material at the openings wherein a chamber pressure, chamber temperature, substrate temperature, a process gas chemistry, a process gas flow rate, a target material, an ICP power, substrate position, a target power, or a substrate bias power or a combination thereof is adjusted to change the process from the NND process to the LND process (Claim 64), the LND bottom surface deposition rate is not discussed (Claims 67, 68), the LND processing time is not discussed (Claim 69), the LND processing time being greater than approximately 150 seconds and less than approximately 250 seconds is not discussed (Claim 70), the power to the target is not discussed (Claims 73, 74), the pressure during the LND is not discussed (Claim 77), the LND process gas is not discussed (Claim 78), the LND process gas being an inert gas is not discussed (Claim 79), the LND process depositing a seed layer is not discussed (Claim 81), the LND process to repair a seed layer is not discussed (Claim 82), the LND process to repair a barrier layer is not discussed (Claim 83), the transfer system is not discussed (Claim 85), a second chamber for LND is not discussed (Claim 87) and the second chamber for LND is not discussed (Claim 89).

Regarding the wafer table being cooled to a temperature of approximately -30 degrees C (Claim 43), Yasar et al. teach the wafer and thus the wafer table to about -30 degrees C. (Paragraph 0039; Paragraph 0032)

Regarding the pressure (Claim 43), Yasar et al. teach switching from high pressure deposition to lower pressure etch cycles. (See Paragraph 0048) The deposition pressure can range from 1 to 150 mTorr. (See Paragraph 0046) If the

deposition is performed at the high end of the range the etch pressure would be lower. (See Paragraph 0048) If deposition is still occurring during the etch cycle because of the reduced power the thermalization of the sputtered material is desired and the pressure should be 50-150 mTorr. (See Paragraph 0046)

Regarding the target power level (Claim 43), Yasar et al. teach the target power is substantially reduced during the etching therefore suggesting approximately 100 W to approximately 1500 W. (See Paragraph 0035)

Regarding claim 43, Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27) Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18)

Regarding the deposition rate (Claims 43, 45-47), Yasar et al. teach the NND rate to be 0 nm/minute since the power to the target can be stopped or can be reduced to close to 0 by reducing the power to the target (See Paragraph 0035)

Regarding claim 64, Yasar et al. teach deposition and etching. (See Yasar et al. discussed above) Yao et al. discusses avoiding deposition at the field regions. (See Yao et al. discussed below) Yao et al. teach a method of operating a deposition system comprising positioning a patterned substrate on a wafer table within a processing chamber. (See Fig. 1) Creating a high density plasma in the processing chamber wherein the high density plasma comprises ions of coating material and a large number of process gas ions. (Column 3lines 25-42; Column 6 lines 12-26) Exposing the patterned substrate to the high-density plasma. Performing a Low Net Deposition

(LND) process wherein a target and substrate bias power is adjusted to establish an LND deposition rate, the LND deposition rate comprising an ultra-low deposition rate in a field area of the patterned substrate. Depositing material into features of the patterned substrate while producing substantially no overhanging material at feature openings. (Column 4 lines 7-18; Column 5 lines 44-68; Column 6 lines 1-11)

Regarding claims 67, 68, Yao et al. teach the LND deposition rate to the higher in the trench. (Column 6 lines 22-26)

Regarding claim 69, Yasar et al. teach that deposition can be between 10 seconds and 500 seconds. (See Fig. 5)

Regarding claim 70, Yasar et al. teach the processing time to be greater than approximately 150 seconds depending on the number of etch and deposition steps. (See Fig. 5)

Regarding claims 73, 74, Yasar et al. teach the target power being from 1kw and less than 0.5 kW. (See Paragraph 0006)

Regarding claim 77, Yasar et al. teach the pressure during deposition can be 50 mTorr. (See Table I) The pressure can be adjusted during the cycle. (Paragraph 0042)

Regarding claim 78, Yasar et al. teach the flowing an inert gas into the process chamber. (Paragraph 0034)

Regarding claim 79, Yasar et al. teach the gas can be argon. (Paragraph 0034)

Regarding claims 81, 82, 83, Yasar et al. teach depositing a seed layer or repairing a seed layer or a barrier layer. (Paragraph 0003, 0004, 0011)

Regarding claim 85, Yasar et al. teach utilizing a transfer system to transfer a substrate to a deposition system. (Paragraph 0007)

Regarding claim 86, Yasar et al. suggest depositing a barrier layer and then a seed layer on a substrate. (See Paragraph 0003; 0004) Yasar et al. suggest utilizing the deposition and etch process to deposit these layers. (See Paragraph 0011)

Regarding claim 87, Yasar et al. teach utilizing a second chamber for a second LND process. (See Paragraph 0007)

Regarding claim 88, Yasar et al. suggest depositing a barrier layer and then a seed layer on a substrate. (See Paragraph 0003; 0004) Yasar et al. suggest utilizing the deposition and etch process to deposit these layers. (See Paragraph 0007)

Regarding claim 89, Yasar et al. teach utilizing a second chamber for a second NND process. (See Paragraph 0007)

The motivation for utilizing the features of Yasar et al. is that it allows for filling of the high aspect ratio holes. (See Abstract)

The motivation for utilizing the features of Yao et al. is that it allows for filling trenches and vias. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the features of Yasar et al. in combination with the features of Yao et al. because it allows for filling high aspect ratio holes.

Claims 60 and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasar et al. in view of Yao et al. as applied to claims 43, 45-49, 53, 55, 57-59, 61,

62, 84 and 97 and 64, 67-70, 73, 74, 77-79, 81-83, 85-89 above, and further in view of Konishi et al. (Japan 09-360040).

The differences not yet discussed is the metal gas. (Claims 60, 80)

Regarding claims 60, 80, Konishi et al. teach utilizing an organometallic gas during sputtering comprising Titanium. (See Konishi Abstract; Machine Translation)

The motivation for utilizing the features of Konishi et al. is that it allows for controlling the composition of the deposited film. (See Konishi et al. Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the features of Konishi et al. because it allows for controlling the composition of the deposited film.

Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasar et al. in view of Yao et al. as applied to claims 43, 45-49, 53, 55, 57-59, 61, 62, 84 and 97 and 64, 67-70, 73, 74, 77-79, 81-83, 85-89 above, and further in view of Gopalraja et al. (U.S. Pat. 6,274,008).

The differences not yet discussed is punch through. (Claim 63)

Regarding claim 63, Gopalraja et al. teach punching through the bottom layer. (Column 13 lines 20-22)

The motivation for utilizing the features of Gopalraja et al. is that it allows for enhancing sidewall coverage. (Column 13 lines 22-23)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized the features of Gopalraja et al. because it allows for enhancing sidewall coverage.

Claims 98-102, 108 and 109 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yao et al. (U.S. Pat. 6,051,114) in view of Yasar et al. (US PGPUB 2003/0034244 A1).

Regarding claim 98, Yao et al. teach a method of operating a deposition system comprising positioning a patterned substrate on a wafer table within a processing chamber. The patterned substrate has features such as a field area, a sidewall and a bottom surface. (See Fig. 1; (See Fig. 3A-3C; Column 5 lines 36-43) Creating a high density plasma in the processing chamber wherein the high density plasma comprises ions of coating material and a large number of process gas ions. (Column 3lines 25-42; Column 6 lines 12-26) Exposing the patterned substrate to the high-density plasma. Performing a Low Net Deposition (LND) process wherein a target and substrate bias power is adjusted to establish an LND deposition rate. (Column 4 lines 7-18; Column 5 lines 44-68; Column 6 lines 1-27) The performing of the LND process step includes depositing material onto the field area at a deposition rate of not more than 30 nanometers per minute while depositing or etching material, or a combination thereof, on the sidewall or the bottom surface or a combination thereof and thereby producing substantially no overhanging material at feature openings. Yao et al. teach controlling parameters to establish a net zero deposition rate on a field area of a substrate. (See Fig. 3B; Column 6 lines 12-27) Yao et al. teach simultaneous bombardment with ions and deposition. (Column 6 lines 12-18) Yao teach adjusting a power output level for a DC source to a target to an LND target power level greater than approximately 1000 W

and less then approximately 3000 W. (i.e. P=V * I; 800V * 2 Amps = 1600 W) (Column 9 lines 45-47)

Regarding claim 101, Yao et al. teach the gas to be used is an inert gas. (Column 3 lines 52-56)

The differences between Yao et al. and the present claims is that the processing chamber being at a chamber pressure of greater than approximately 20 mTorr and less than approximately 130 mTorr is not discussed (Claim 98), adjusting an ICP source to provide an LND ICP power level of greater than approximately 3000 W and less than 6000 W is not discussed (Claim 98), the bias power to the substrate is not discussed (Claim 99), the wafer table temperature is not discussed (Claim 100), the NND process is not discussed (Claim 102), the performing the LND process step further includes a wafer table temperature to approximately -30 degrees Celsius and the deposition system further comprises a gas supply system coupled to the processing chamber and the method further comprising flowing a first process gas into the processing chamber during at least a portion of the LND process step, wherein the first process gas comprises an inert gas, a nitrogen containing gas, an oxygen containing gas, or a metal containing gas or a combination thereof is not discussed (Claim 108), and performing a No Net Deposition process step after performing the LND process step by adjusting the ICP source to provide an NND ICP power level of greater than approximately 1000 w and less than 10,000 w and adjusting the power output level for the DC source coupled to the target to an NND target power level greater than approximately 100 w and less than approximately 1500 w to establish an NND deposition rate for

depositing material onto the field area, where the NND deposition rate is greater than approximately -10 nanometers per minute (nm/min) and less than 10 nanometers per minute (nm/min) while material is deposited onto the sidewall and while material is deposited and etched on the bottom surface, thereby producing substantially no overhanging material at the feature opening is not discussed (Claim 109).

Regarding claim 98, Yasar et al. teach depositing at a pressure of 50 to 120 mTorr. (See Table I)

Regarding claim 98, Yasar et al. teach operating an ICP source at 1-7 KW. (See Table I)

Regarding claim 99, Yasar et al. teach a bias power of 0-200 W to the substrate. (See Table I)

Regarding claim 100, Yasar et al. teach the temperature of the substrate to be about -30 degrees C. (Paragraph 0039; Paragraph 0032)

Regarding claim 102, Yasar et al. teach a method of operating a deposition system by positioning a patterned substrate on a wafer table within a processing chamber. (See Figs. 3, 3A, 3B) Creating a high density plasma in the processing chamber wherein the high density plasma comprises a large concentration of metal ions and a large number of process gas ions. Exposing the patterned substrate to the high density plasma. Performing a NO Net Deposition (NND) process, wherein a target power or a substrate bias power or a combination thereof, is adjusted to establish an NND deposition rate, the NND deposition rate comprising an NND field deposition rate, an NND sidewall deposition rate, or an NND bottom surface deposition rate or a

combination thereof. Processing the patterned substrate using the NND process, thereby depositing material on sidewalls of features of the patterned substrate or bottom surfaces of features of the patterned substrate, or a combination thereof, wherein a chamber pressure, chamber temperature, substrate temperature, a process gas chemistry, a process gas flow rate, a target material, an ICP power, substrate position, a target power, or a substrate bias power, or a combination thereof, is adjusted during the NND process. (Paragraph 0035; Paragraph 0042; Paragraph 0043) The target power is substantially reduced therefore suggesting approximately 100 W to approximately 1500 W. (See Paragraph 0035) Yasar et al. teach utilizing an ICP power of 3000 W. (See Table II) Yasar et al. teach that the deposition rate can be 0 or lower since the deposition can be stopper. (Paragraph 0035)

Regarding claim 108, Yasar et al. teach the wafer and thus the wafer table to about -30 degrees C. (Paragraph 0039; Paragraph 0032) Yasar et al. teach the sputtering gas can be argon gas and nitrogen. (Paragraph 0034) Yasar et al. teach a gas supply. (See Figs. 3, 3A)

Regarding claim 109, Yasar et al. teach a method of operating a deposition system by positioning a patterned substrate on a wafer table within a processing chamber. (See Figs. 3, 3A, 3B) Creating a high density plasma in the processing chamber wherein the high density plasma comprises a large concentration of metal ions and a large number of process gas ions. Exposing the patterned substrate to the high density plasma. Performing a NO Net Deposition (NND) process, wherein a target power or a substrate bias power or a combination thereof, is adjusted to establish an

NND deposition rate, the NND deposition rate comprising an NND field deposition rate, an NND sidewall deposition rate, or an NND bottom surface deposition rate or a combination thereof. Processing the patterned substrate using the NND process, thereby depositing material on sidewalls of features of the patterned substrate or bottom surfaces of features of the patterned substrate, or a combination thereof, wherein a chamber pressure, chamber temperature, substrate temperature, a process gas chemistry, a process gas flow rate, a target material, an ICP power, substrate position, a target power, or a substrate bias power, or a combination thereof, is adjusted during the NND process. (Paragraph 0035; Paragraph 0042; Paragraph 0043) Yasar et a. teach the NND time can be greater than approximately 150 seconds depending on the number of etch and deposition steps. (See Fig. 5) The target power is substantially reduced therefore suggesting approximately 100 W to approximately 1500 W. (See Paragraph 0035) Yasar et al. the ICP power can be 3000 W. (See Table II) Yasar et al. teach that the no net deposition rate can be 0 or lower since the deposition can be stopper. (Paragraph 0035)

The motivation for utilizing the features of Yasar et al. is that it allows for filling of the high aspect ratio holes. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Yao et al. with the features of Yasar et al. because it allows for filling high aspect ratio holes.

Claims 103-107, 110 and 111 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasar et al. (U.S. PGPUB. 2003/0034244 A1) in view of Yao et al. (U.S. Pat. 6,051,114).

Regarding claim 103, Yasar et al. teach a method of operating a deposition system by positioning a patterned substrate on a wafer table within a processing chamber. (See Figs. 3, 3A, 3B) Creating a high density plasma in the processing chamber wherein the high density plasma comprises a large concentration of metal ions and a large number of process gas ions. Exposing the patterned substrate to the high density plasma. Performing a NO Net Deposition (NND) process, wherein a target power or a substrate bias power or a combination thereof, is adjusted to establish an NND deposition rate, the NND deposition rate comprising an NND field deposition rate, an NND sidewall deposition rate, or an NND bottom surface deposition rate or a combination thereof. Processing the patterned substrate using the NND process, thereby depositing material on sidewalls of features of the patterned substrate or bottom surfaces of features of the patterned substrate, or a combination thereof, wherein a chamber pressure, chamber temperature, substrate temperature, a process gas chemistry, a process gas flow rate, a target material, an ICP power, substrate position, a target power, or a substrate bias power, or a combination thereof, is adjusted during the NND process. (Paragraph 0035; Paragraph 0042; Paragraph 0043) The target power is substantially reduced therefore suggesting approximately 100 W to approximately 1500 W. (See Paragraph 0035) Yasar et al. teach utilizing an ICP power

of 3000 W. (See Table II) Yasar et al. teach that the deposition rate can be 0 or lower since the deposition can be stopper. (Paragraph 0035)

Regarding claim 104, Yasar et al. teach the target power is substantially reduced therefore suggesting approximately 500 W to approximately 1500 W. (See Paragraph 0035)

Regarding claim 105, Yasar et al. teach the temperature of the substrate to be about -30 degrees C. (Paragraph 0039; Paragraph 0032)

Regarding claim 106, Yasar et al. teach utilizing argon. (Paragraph 0035)

Regarding claim 107, Yasar et al. teach performing a low net deposition process by utilizing an ICP power greater than 1000 W and less than 3000 W. (See Table I)

The difference between Yasar et al. and the present claims is that the power to the target being greater than approximately 1000 W and less than approximately 3000 W is not discussed (Claim 107), the performing the NND process step further includes adjusting a wafer table temperature to approximately-30° Celsius; and the deposition system further comprises a gas supply system coupled to the processing chamber and the method further comprises flowing a first process gas into the processing chamber during at least a portion of the NND process step, wherein the first process gas comprises an inert gas, a nitrogen-containing gas, an oxygen-containing gas, or a metal-containing gas, or a combination thereof is not discussed (Claim 110) and performing a Low Net Deposition (LND) process step after performing the NND process step by adjusting the ICP source to provide an LND ICP power level of greater than approximately 3000 w and less than 6000 w and adjusting the power output level for the

DC source coupled to the target to an LND target power level greater than approximately 1000 w and less than approximately 3000 w to establish an LND deposition rate for depositing material onto the field area, where the LND deposition rate is less than 30 nanometers per minute (nm/min) while material is deposited and etched on the sidewall or the bottom surface, or a combination thereof, thereby producing substantially no overhanging material at the feature opening (Claim 111).

Regarding claim 107, Yao et al. teach adjusting a power output level for a DC source to a target to an LND target power level greater than approximately 1000 W and less then approximately 3000 W. (i.e. P=V * I; 800V * 2 Amps = 1600 W) (Column 9 lines 45-47)

Regarding claim 110, Yasar et al. teach the wafer and thus the wafer table to about -30 degrees C. (Paragraph 0039; Paragraph 0032) Yasar et al. teach the sputtering gas can be argon gas and nitrogen. (Paragraph 0034) Yasar et al. teach a gas supply. (See Figs. 3, 3A)

Regarding claim 111, Yasar et al. teach a method of operating a deposition system by positioning a patterned substrate on a wafer table within a processing chamber. (See Figs. 3, 3A, 3B) Creating a high density plasma in the processing chamber wherein the high density plasma comprises a large concentration of metal ions and a large number of process gas ions. Exposing the patterned substrate to the high density plasma. Performing a Low Net Deposition (LND) process, wherein a target power or a substrate bias power or a combination thereof, is adjusted to establish an LND deposition rate, the LND deposition rate comprising an LND field deposition rate,

an LND sidewall deposition rate, or an LND bottom surface deposition rate or a combination thereof. Processing the patterned substrate using the LND process, thereby depositing material on sidewalls of features of the patterned substrate or bottom surfaces of features of the patterned substrate, or a combination thereof, wherein a chamber pressure, chamber temperature, substrate temperature, a process gas chemistry, a process gas flow rate, a target material, an ICP power, substrate position, a target power, or a substrate bias power, or a combination thereof, is adjusted during the LND process. (Paragraph 0035; Paragraph 0042; Paragraph 0043) Yasar et a. teach the LND time can be greater than approximately 150 seconds depending on the number of etch and deposition steps. (See Fig. 5) The target power is substantially reduced therefore suggesting approximately 100 W to approximately 1500 W. (See Paragraph 0035) Yasar et al. the ICP power can be 3000 W. (See Table II) Yasar et al. teach that the low net deposition rate can be 0 or lower since the deposition can be stopper. (Paragraph 0035)

The motivation for utilizing the features of Yao et al. is that it allows for filling integrated circuits. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Yasar et al. by utilizing the features of Yao et al. because it allows for filling integrated circuits.

Response to Arguments

Applicant's arguments filed April 13, 2009 have been fully considered but they are not persuasive.

In response to the argument that the prior art of record does not teach depositing films without overhangs by a simultaneous IPVD and etching process, it is argued that Yao et al. teach that power parameters can be tailored to achieve sputtering of metal while simultaneously removing the metal layer formed on the field by bombardment with ions so that the build up of metal is limited to prevent bridging of metal over the trench. (See Yao et al. discussed above)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 571-272-1340. The examiner can normally be reached on M-Th with every Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rodney G. McDonald/
Primary Examiner, Art Unit 1795

Rodney G. McDonald
Primary Examiner
Art Unit 1795

RM
June 25, 2009